HIGH ASPECT RATIO SiLICON NANOFABRICATION (HARSiN) TECHNOLOGY

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A simplified process to fabricate high aspect ratio nanostructures in silicon combining electron beam lithography and deep reactive ion etching (DRIE) is presented. A stable process (HARSiN) has been developed without the need for complicated resist/hard mask processing or complex dry etch technologies. This is achieved using commercially available ZEP520A resist from Nippon Zeon Co., Ltd which allows high resolution ebeam imaging (≤50nm) as well as affords high plasma etch resistance to a continuous room temperature carbon/fluorine DRIE Si etch chemistry developed in this work. Using this simplified lithography/etch process sequence, high aspect ratio (>14:1) silicon nanometer structures are reported for nanotechnology applications, which are reviewed in this paper.

Compared to state of the art processes, HARSiN offers several advantages. The use of ZEP520A removes the requirement for multilevel conventional resist/hard mask levels [1] and chemically amplified resists (CAR) [2]. This advantage is combined with a carbon/fluorine etch chemistry with a selectivity performance reported here that is an order of magnitude greater than traditional chlorine/bromine etch chemistries (1:1) used in microelectronics processing [3]. In addition, a continuous room temperature etch/passivation recipe has been developed using this etch chemistry. This represents a significant simplification to processes such as cryogenic processing and Bosch etching where for the latter, etching and passivation is cycled resulting in often unwanted sidewall scalloping and undercut, which limits the minimal size of the features [4].

To demonstrate the HARSiN process characteristics, SEM shots of fabricated 2D lattice design consisting of test arrays of honeycomb columns, holes and trenches are shown in Fig. 1. The total design area was 5000µm (L) x 12µm (W) with typical dimensions ranging from 200nm to 50nm for both pillar diameters and trench widths, and with 200nm hole diameters.

The process used for these structures involved spinning ZEP520 at 4000rpm for 60s followed by a 5min soft-bake at 180°C. A 50kV electron beam exposure using a Jeol JBX6000 system for doses from 100 to 150µC/cm with 100pA beam current were investigated in this work and is reported. Post exposure processing followed using a 40s ZED-N50 development step and a subsequent 40s IPA rinse. The Si etch was carried out using an Inductively Coupled Plasma (ICP) etch system manufactured by Surface technology Systems (STS^{HRM}). During the etch process, the Si sidewalls were coated with polymer from C4F8 dissociation while the bottom of the exposed features was etched by ion bombardment which prevented passivation build up. The continuous etch/ passivation recipe used in this work resulted in vertical sidewall, with no undercut (under-etch bellow the mask) or scalloping, see high resolution SEM Fig. 2 & 3. Selectivity (~10:1) between Si and the ZEP resist is reported using a Si etch rate ~1µm/min. A summary of the HARSiN process performance is provided in Table I.

In conclusion, a stable and simplified process for fabricating silicon nanostructures is reported. The potential applications of the technology will be discussed and include Si based 2D lattice Photonic

Bandgap crystal devices, controlled honeycomb nanorod coatings for microfluidics, nanoelectrode arrays for nano-gap resonator and Si master stamps for nanoimprint lithography (NIL).

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Table I: Summary of the HARSiN technology

Process	*HARSiN*
Chemistry	SF6/C4F8
Resist	ZEP520
Resist Selectivity	~10:1
Aspect Ratio	>14:1
Undercut	Nominally zero
Feature Size (min)	60nm
Si Etch Rate	~1µm/min

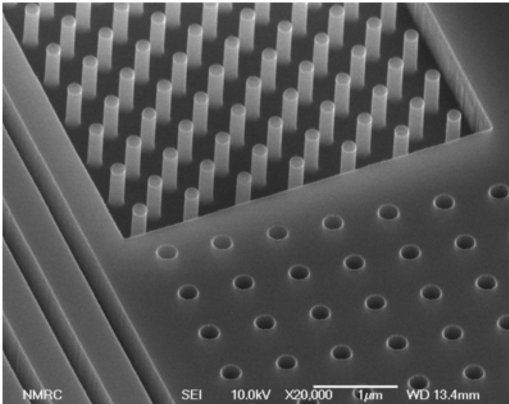

Figure 1: SEM of HARSiN technology.

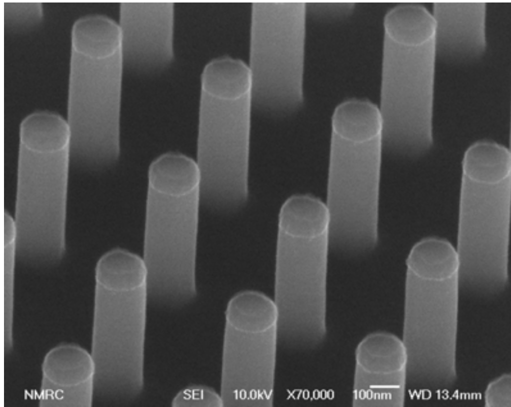

Figure 2: High resolution SEM (40° tilt) of arrays of 850nm high, 170nm diameter pillars.

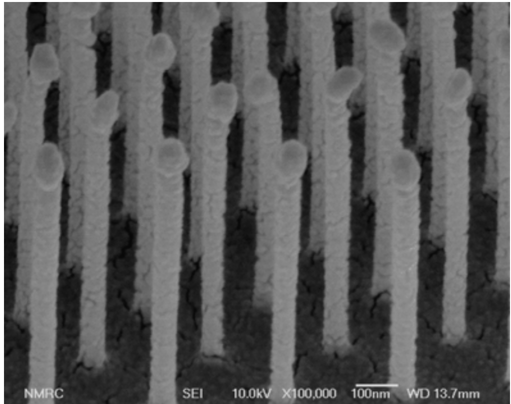

Figure 3: High resolution SEM (40° tilt) of arrays of 850nm high, 65nm diameter Si pillars. Sidewall roughness comes from a thin gold coating to get better SEM imaging.