Silicon Sacrificial Layer Dry Etching (SSLDE) for free-standing RF MEMS architectures

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ABSTRACT

A novel Silicon Sacrificial Layer Dry Etching (SSLDE) technique using sputtered amorphous or LPCVD polycrystalline silicon as sacrificial layers and a dry fluorine-based (SF_6) plasma chemistry as releasing process is reported with a detailed experimental study of the release etching step. The process is capable of various applications in surface micromachining process, and can be applied in fabricating RF MEMS switches, tunable capacitors, high-Q suspended inductors and suspended-gate MOSFETs. The developed SSLDE process can release metal suspended beams and membranes with excellent performance in terms of etch rate (up to 15μm/min), Si:SiO_2 selectivity and is fully compatible with standard MEMS processing equipment and CMOS post-processing.

INTRODUCTION

Among various surface micromachining techniques developed and reported in recent years, the polysilicon process, which involves silicon dioxide sacrificial layer wet etch followed by supercritical carbon dioxide drying process [1], and the use of organic sacrificial layers released in oxygen plasma [2, 3] have been successfully employed. However, these processes suffer from some inherent problems like stiction related to wet etching [4], or low etch rates (largely under 1μm/min for organic layers), that make the process not very efficient when necessary to release relatively large membranes as required for RF MEMS tunable capacitors.

In this work, we report a detailed study of Silicon Sacrificial Layer Dry Etching (SSLDE), with sputtered amorphous or LPCVD polycrystalline silicon used as sacrificial layers and dry fluorine-based (SF_6) plasma chemistry as releasing process. SSLDE process can be successfully adapted and applied for the fabrication of RF MEMS switches, tunable capacitors, high-Q suspended inductors and suspended-gate MOSFETs [5, 6].

The key challenge in SSLDE was to improve the releasing step by obtaining a high aspect ratio (length-to-thickness ratio), maximal etch rate of the sacrificial layer and high selectivity to the insulator layer (SiO_2). The experiments have been performed in a high-density ICP reactor (Alcatel 601E) taking advantage of the independent control of radicals, ion flux and chuck temperature. Etching was performed using fluorine-based chemistry (SF_6), which is commonly used to achieve deep anisotropic Si etching with high etch rate, high uniformity (+/- 5%) and high Si:SiO_2 selectivity (more than 150:1). However, by increasing chemical etching and limiting physical etching, underetch of thin silicon layer with high selectivity to SiO_2 can also be performed in ICP equipment.

FABRICATION PROCESS

In this section, the surface micromachining process developed at EPFL for RF MEMS tunable capacitor fabrication is presented. It is a full-dry process because all steps involving etching included the releasing step are essentially dry. A cross section of a RF MEMS capacitor fabricated with SSLDE is reported in Fig. 1(a): it uses two metal layers with two insulator barriers and a sacrificial amorphous silicon layer in-between. The first aluminum metal layer is sputtered and patterned using chlorine-based plasma chemistry. Then, a LTO LPCVD SiO_2 diffusion barrier layer is deposited to improve smoothness of aluminum structures. Next, a thick amorphous silicon sacrificial layer is sputtered and patterned to obtain a multi-air-gaps structure. The second LTO LPCVD SiO_2 diffusion barrier layer and aluminum metal layer are respectively deposited and sputtered. Then, the aluminum metal layer is patterned using the same process as for the first aluminum layer whereas LTO LPCVD SiO_2 layer is patterned with C_xF_y-based plasma chemistry to an access to the sacrificial layer. Finally, suspended metal membranes are released in a fluorine-based chemistry with high selectivity to SiO_2. Fig. 1(b) depicts a typical tunable capacitor fabricated with this process. SSLDE process has also been successfully adapted to achieve suspended gate devices with metal-over-gate architectures. In suspended-gate MOSFETs, the polysilicon layer of standard CMOS process is used as sacrificial layer.

RELEASING STEP INVESTIGATIONS

In the following, we present a detailed experimental study concerning the influence of the most relevant etching parameters and design parameters: (i) process time dependency, (ii) SF_6 flow rate, (iii) pressure, (iv) chuck temperature, (v) ICP source power, (vi) opening feature size of the structures and (vii) silicon sacrificial layer thickness. Subsequently, their impact on the: (i) silicon etch rate, (ii) silicon dioxide etch rate and (iii) Si:SiO_2 selectivity are reported.

To investigate sacrificial layer etching, the top aluminum metal layer was not deposited so that observations can be done over the top transparent LTO LPCVD SiO_2 layer using a conventional optical microscope. Silicon dioxide thickness has been measured beside the membrane using a spectro-reflectometer. Fig. 2 depicts a cross section of the sacrificial layer and SiO_2 layer shape evolution during the releasing step.

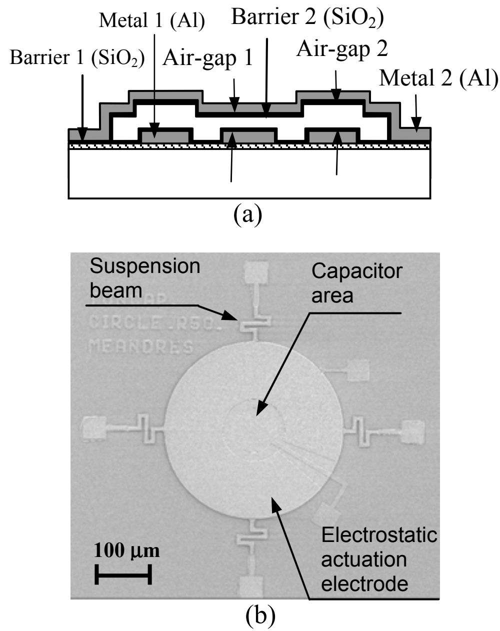

Figure 1: (a) Cross section of RF MEMS tunable capacitors design with double air-gap and separated electrostatic actuation resulting in increased capacitance tuning range [7], (b) SEM picture of a typical RF MEMS capacitor fabricated with SSLDE process. Suspension beams were designed with meanders to decrease the equivalent spring constant. The RF capacitor has a 100µm diameter and a 1µm air-gap.

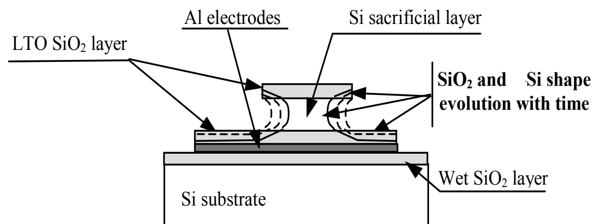

Figure 2: Illustration of SiO_2 and sacrificial layer shape evolution with process time.

Underetch length time dependency

The releasing using a 1µm a-Si sacrificial layer has been carried out up to 450µm etched horizontal dimension, with various combinations of process parameters resulting in a very uniform etch rate that can be as high as 15µm/min (see Fig. 3). From *Process 1 to 3*, SF_6 flow rate is increased (100, 300, 500sccm) and leads to increase the number of fluorine radicals available in chemical reaction resulting in higher etch rate of silicon. Underetch length increases rapidly (from 3µm/min to 7µm/min depending on SF_6 flow rate) and linearly with process time. Contrary to deep anisotropic etching where etch rate decrease with depth, underetch rate of thin silicon layer is constant over a large length; it is pointed out that reactant flux in extremely thin gaps is sufficient to (1) enhance chemical reaction and (2) evacuate volatile products. We therefore conclude that physical reaction (i.e.: ions bombardment) in deep etching is a factor of etching limitation as process time. After plasma settings optimization, very high Si etch rate and high selectivity on SiO_2 were performed with *Process 4* (see also Fig. 9 inset).

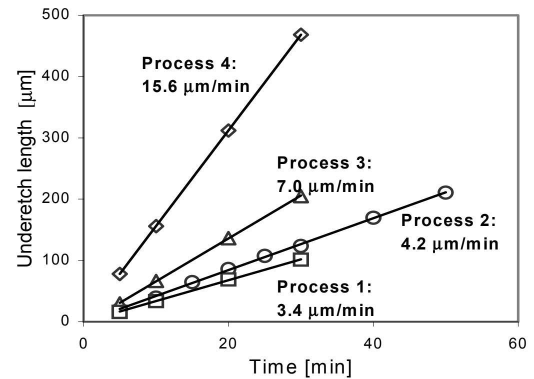

Figure 3: Underetch of 1µm a-Si sacrificial layer as a function of time for different processes.

Pressure

Process pressure has a great impact on overall etching results, it is known to have a large influence on plasma features such as the ratio ions/neutrals, sheath potential, energy of ions reaching the surface and chemical kinetics. Higher pressure leads to increase the number of fluorine radicals available in chemical reaction resulting in higher etch rate of silicon. The releasings are done at room temperature (20°C) with a source power of 1500W and a SF_6 flow rate of 300sccm by changing the process pressure in the range of 3-18Pa. It can be seen in Fig. 4 that a-Si, polySi and SiO_2 etch rate increase as a function of reactor pressure with a threshold around 10 Pa. This is probably due to the chemical reaction saturation; indeed, underetch rate cannot increase indefinitely and is limited by reactant products. However, higher pressure also increases the collision ion/neutral, thereby reducing ions directionality and ions energy. It might also explain the SiO_2 etch rate slope down observed around 10 Pa.

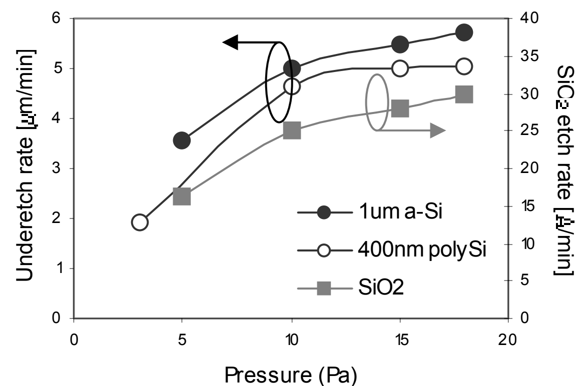

Figure 4: Sacrificial layer and silicon dioxide etch rate as a function of pressure

ICP source power

Increasing ICP source power leads to extend the Electron Energy Distribution Function (EEDF) and therefore, a larger number of electrons with high energy are available for dissociation and ionization. Evolution of sacrificial layer and silicon dioxide etch rate is shown in Fig. 5. It is found that increasing ICP source power increases SiO_2 and sacrificial layer etch rate. A threshold is observed around 1500W for the 200nm polySi sacrificial layer and around 2500W for the 1µm a-Si sacrificial layer. This is also due to the saturation of reactant species, which depends on thickness of the sacrificial layer and source power. In fact, four fluorine atoms react with one silicon atom to form SiF_4 molecule, which is a volatile product at room temperature. SiF_4 molecules are then desorpted from the surface and pumped away.

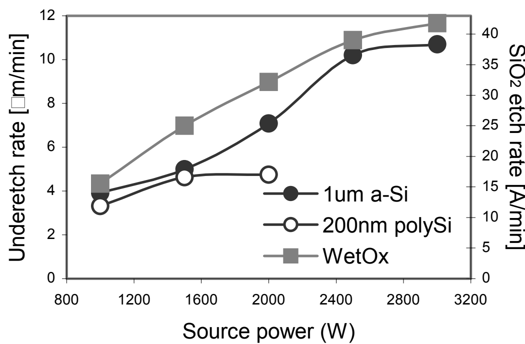

Figure 5: Sacrificial layer underetch rate and silicon dioxide etch rates as a function of source power.

Chuck temperature

The chuck temperature is controllable and influence underetch rate and Si:SiO_2 selectivity. The influence of temperature on the etch process, with an experimental range of -110°C up to 40°C for 30min etch duration, is reported in Fig. 6. It is pointed out that chuck temperature during etching plays a crucial role in reducing silicon dioxide etch rate, while silicon etch rate appears to have a maximum peak close to 0°C. This remark is important for suspended-gate MOSFET, where a high quality gate oxide should remain after releasing. By decreasing the temperature, we show that the silicon dioxide etch rate is significantly reduced without disturbing to much the releasing. These results show clearly that SiO_2 reaction with fluorine was suppressed by lowering chuck temperature. A maximum peak around 0°C was observed for both sacrificial layers (a-Si and polySi). The reason of high etch rate at 0°C is not known at the present time. This is not unexpected since etch rate depends on species sticking probabilities and often changes with surface temperature. The cryogenic cooling advantage is found in the selectivity with respect to silicon dioxide. Temperature is an independent parameter, which control silicon dioxide etch rate without decreasing underetch too much. The chuck temperature is therefore a crucial parameter and special attention must be done when releasing silicon sacrificial layer in order to optimized underetch rate.

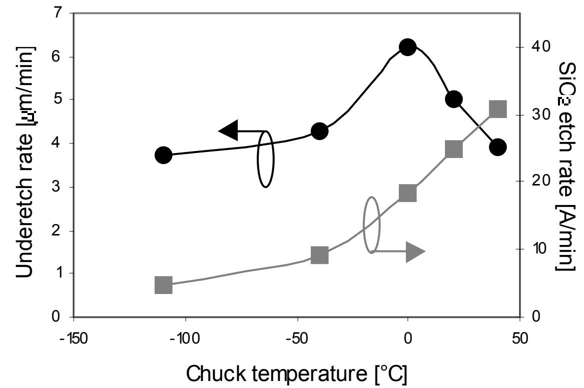

Figure 6: 1µm amorphous silicon (a-Si) and silicon dioxide etch rates versus chuck temperature.

Feature size

Test cells have been designed to study the releasing with the opening area of etching. It consists of trenches with opening sizes from 2µm to 500 µm. Fig. 7 shows the relationship between etch rate and opening size. The etch duration is 30min, source power, bias power, pressure, SF_6 flow rate and chuck temperature are respectively 1500W, 0W, 10Pa, 300sccm and 20°C. Feature size of the structure has been found to have no influence on underetch rate and experimental results show that no Aspect Ratio Dependent Etching (ARDE) effect occurs in lateral etching of silicon unlike deep RIE etching. Taking advantage of this late remark, SSLDE free-standing RF MEMS architecture can be design with 2x2µm^2 or 5x5µm^2 etch holes to reduce the releasing process time.

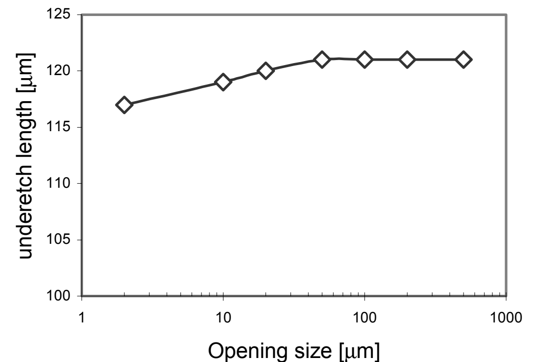

Figure 7: Underetch length of 1µm a-Si sacrificial layer for different opening sizes plotted with a logarithmic scale.

Silicon sacrificial layer thickness

Underetch rate (using *Process 2*) was investigated for different sacrificial materials thickness and is reported in Fig. 8. Underetch rate is constant over a large range of sacrificial layer thickness. This late remark is important for RF MEMS tunable capacitor, where differential air-gaps of sacrificial layer are needed. In addition, SSLDE process is therefore very efficient to release very thin polySi sacrificial layer as required for suspended-gate MOSFETs and to release thick a-Si sacrificial layer as required for RF capacitor.

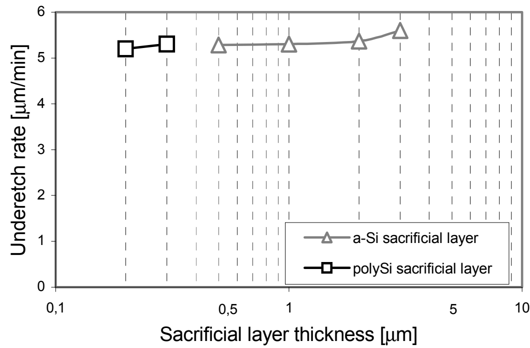

Figure 8: Underetch rate versus thickness of polycrystalline and amorphous silicon plotted with logarithmic scale.

Silicon dioxide under membranes

To better understand silicon dioxide etching under a membrane, a 450µm^2 membrane has been removed to access the first LTO SiO_2 diffusion barrier layer and is thickness has been measured using a spectro-reflectometer. A typical silicon dioxide profile under the released membrane is reported in Fig. 9. We show that SiO_2 etch rate depends on exposure time to plasma since etch rate under membrane is constant (16A/min) and on ions flux since etch rate is higher beside membrane (22A/min). Moreover, Fig. 9 inset depicts oxide thickness beside membranes as a function of process time for different processes. From *Process 1 to 3*, SF_6 flow rate is increased and leads to increase chemical reaction with silicon dioxide. The *Process 4* shows that fluorine reaction with silicon dioxide is frozen by lowering chuck temperature at -110°C.

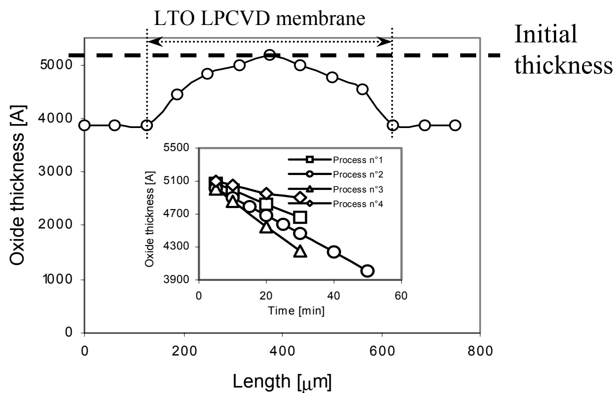

Figure 9: Silicon dioxide profile under membrane after releasing with Process 2. Inset: oxide etch rate versus process time for different recipes.

Optimization process

Based on the previous study of SSLDE, several recipes have been processed in order to find out optimal process parameters. This study has emphasized the fact that temperature plays an important role in this process by limiting silicon dioxide etching. Moreover, the optimal recipe (referenced as *Process 4*) has been found to be independent of the sacrificial layer used (a-Si or polySi) and its thickness. SF_6 flow rate, pressure and source power was respectively set to 500sccm, 18Pa and 3000W whereas chuck temperature was lowered at -110°C. Using this recipe, 15.6µm/min underetch rate with high Si:SiO_2 selectivity (30000:1) has been obtained for different RF MEMS tunable capacitor designs (shape, sacrificial layer thickness). It has been applied to fabricate the RF MEMS tunable capacitor depicts in Fig. 1.

CONCLUSION

In conclusion, the developed SSLDE process can release metal suspended beams and membranes with excellent performance in terms of etch rate (up to 15µm/min), Si:SiO_2 selectivity (30000:1) and is fully CMOS compatible. The advantage of this process has been found in its simplicity and based on its flexibility, it can be used to design a wide range of microsystems. Particularly, it is extremely attractive for RF MEMS tunable capacitors and capacitive switches co-integrated with CMOS. Using this process, it is now possible to release very large capacitor (up to 500 µm) in a few minutes and is expected to contribute in making surface micromachining more competitive and convenient.

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